CLAIMS

1. A signal processing circuit comprising:

data reading out means for reading out data comprising user blocks in the packet and/or link blocks in the connection blocks;

a buffer for successively storing the data which are read out;

user block judging means for judging as to whether the read out data are desired user blocks or not;

address pointer generating means for generating an address pointer on the basis of the judgment result from the user block judging means; and

system control means for controlling to maintain the position of the address pointer at a position in the buffer where the link block is written in prior and to overwrite the data which were read out this time onto the data of link block which are previously written in into the buffer.

2. A signal processing circuit as defined in claim 1, wherein

there is provided block ID detecting means which detects the block ID while successively reading out the data.

3. A signal processing circuit as defined in claim 2, wherein

there is provided continuity judging means which defines continuity of blocks on the basis of the block ID.

4. A signal processing circuit as defined in claim 2, wherein

the user block judging means compares the link block ID under being read out and the top block ID, thereby to judge that the block under being read out is a link block until the top block ID of the user block is detected, or compares the user block under being read out and the top block ID of the link block, thereby to judge that the block under being read out is a user block until the top block ID of the link block is detected.

5. A signal processing circuit as defined in claim 3, wherein

the system control means conducts, when it is detected that the block ID is a link block ID in the same connection block or a top block of a desired user block ID when the discontinuity of the block ID is detected by the continuity judging means, a control such that a re-search of a block is not conducted but the reading out of the data conducted as it is.

6. A signal processing circuit as defined in claim 5, wherein:

the system control means judges the direction of

discontinuity of the block ID by comparing the block ID and the block ID immediately before that when the discontinuity of the block ID is detected by the discontinuity judging means, and it is controlled that when the position of the data reading out position has moved to the direction coming close to a desired user block, re-search of a block is not conducted, while when the reading out position of data has moved to the direction different from that coming close to the desired position, or when the block ID and the block ID immediate before the block ID are identical to each other, the re-search of the block is conducted.

7. A signal processing circuit comprising:

data reading out means for reading out data comprising user blocks in the packet and/or link blocks in the connection blocks;

a buffer for successively storing data which are read out;

user block judging means for judging as to whether the read out data are desired user blocks or not; and

data control means for controlling so that the data is converted in its data format and is stored in the buffer.

8. A signal processing circuit comprising:

data reading out means for reading out data comprising user blocks in the packet and link blocks in the connection blocks, which are stored on tracks formed on an optical disc;

a buffer for successively storing the data which are read

out;

user block judging means for judging as to whether the read out data are desired user blocks or not; and

data control means for controlling a distinction information with being added to the data is stored in the buffer, which distinction information which can distinguish whether the data read out as above is user block or a link block on the basis of the judgment result by the user block judging means.